volts. After the ion implant process the mask over the natural transistor is removed in step **53** and the remaining well known standard processes to fabricate an MOS IC are performed.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit of a DRAM cell requiring a reduced output current comprising:

a switch to activate a write operation to said DRAM cell;

a storage capacitor;

a pass transistor to support a read operation out of said DRAM cell being a natural transistor;

a switch to activate a read operation out of said DRAM cell; and

a current source to support the read operation out of said DRAM cell.

2. The circuit of claim **1** wherein said switch to activate a write operation is a transistor.

3. The circuit of claim **1** wherein said natural transistor is a MOS natural transistor.

4. The circuit of claim **3** wherein said natural transistor is a PMOS transistor.

5. The circuit of claim **3** wherein said natural transistor is a CMOS transistor.

6. The circuit of claim **3** wherein said natural transistor is a NMOS transistor.

7. The circuit of claim **1** wherein said current source is a constant current source.

8. A circuit of a multi-level DRAM cell requiring a reduced output current comprising:

a storage capacitor;

a multiplexer having multiple switches to activate a write operation for a specific voltage level to said storage capacitor;

a pass amplifier to support a read operation out of said storage capacitor comprising a natural transistor;

a current source to support the read operation out of said DRAM cell;

a switch to activate a read operation out of said storage capacitor; and

an analog-to-digital converter (ADC) to convert the analog values of said read operation into digital values.

9. The circuit of claim **8** wherein said switches to activate a write operation are transistors.

10. The circuit of claim **8** wherein said switch to activate a read operation is a transistor.

11. The circuit of claim **8** wherein said natural transistor is a MOS natural transistor.

12. The circuit of claim **11** wherein said natural transistor is a PMOS transistor.

13. The circuit of claim **11** wherein said natural transistor is a CMOS transistor.

14. The circuit of claim **11** wherein said natural transistor is a NMOS transistor.

15. The circuit of claim **8** wherein said current source is a constant current source.

16. A method to achieve a two-level DRAM cell requiring a reduced output current, comprising:

providing a capacitor, a transistor as pass transistor, and peripheral circuitry to activate and to drive said DRAM cell comprising switches, a current source and an amplifier;

deploy said capacitor as DRAM storage element; and

deploy a transistor, having a minimal threshold voltage, as pass transistor to sense the charge of said storage capacitor, wherein said charge represents a value of stored information.

17. The method of claim **16** wherein said pass transistor; having a minimal threshold voltage, is a natural transistor.

18. The method of claim **16** wherein said switches are standard transistors.

19. A method to achieve a multi-level DRAM cell requiring a reduced output current, comprising:

providing a capacitor, a transistor as pass transistor, and peripheral circuitry to activate and to drive said DRAM cell comprising a multiplexer containing switches to activate a desired voltage level, a switch to activate a read-out of said DRAM cell, an analog-to-digital converter, a current source, and an amplifier;

deploy said capacitor as DRAM storage element; and

deploy a transistor, having a minimal threshold voltage, as pass transistor to sense the charge of said storage capacitor, wherein said charge represents a value of stored information.

20. The method of claim **19** wherein said pass transistor; having a minimal threshold voltage, is a natural transistor.

21. The method of claim **19** wherein said switches in said multiplexer and said switch to activate the read-out are standard transistors.

22. A method to fabricate a two-level DRAM cell requiring a reduced output current, comprising:

providing a capacitor, a natural transistor as pass transistor, and peripheral circuitry to activate and to drive said DRAM cell comprising standard transistors, a current source and an amplifier;

mask the channel of the natural transistor to avoid any impurities caused by the following ion implant step;

perform ion implant to define threshold voltage of the standard transistors as part of the DRAM cell; and

remove mask from natural transistor and continue standard processes.

23. The method of claim **22** wherein said natural transistor is a PMOS transistor.

24. The method of claim **22** wherein said natural transistor is a CMOS transistor.

25. The method of claim **22** wherein said natural transistor is a NMOS transistor.

26. A method to fabricate a multi-level DRAM cell requiring a reduced output current, comprising:

providing a capacitor, a natural transistor as pass transistor, and peripheral circuitry to activate and to drive said DRAM cell comprising a multiplexer containing transistors to activate a desired voltage level, a transistor to activate a read-out of said DRAM cell, an analog-to digital converter, a current source and an amplifier;

mask the channel of the natural transistor to avoid any impurities caused by the following ion implant step;

perform ion implant to define threshold voltage of the standard transistors as part of the DRAM cell; and

remove mask from natural transistor and continue standard processes.

27. The method of claim **26** wherein said natural transistor is a PMOS transistor.

28. The method of claim **26** wherein said natural transistor is a CMOS transistor.

29. The method of claim **26** wherein said natural transistor is a NMOS transistor.